## CLAIMS

What is claimed is:

1. A method, comprising:

determining that each thread running on a processor has issued a pause instruction; and

reducing power consumption in response to the determination that each thread running on the processor has issued a pause instruction.

2. The method of claim 1, further comprising reducing the frequency of the processor.

3. The method of claim 1, further comprising gating M clock cycles out of every N clock cycles of a processor clock.

4. The method of claim 1, further comprising increasing power consumption after a predetermined time period has elapsed or when an event occurs.

5. The method of claim 1, further comprising lowering processor voltage.

6. The method of claim 1, further comprising running only one thread on the processor.

7. The method of claim 1, further comprising slowing down the processor.

8. A method, comprising:

determining that each thread running on a processor has issued a pause instruction; and

leave a normal mode of operation and entering into a slow mode of operation in response to the determination that each thread running on the processor has issued a pause instruction.

9. The method of claim 8, further comprising reducing processor frequency.

10. The method of claim 8, further comprising gating M clock cycles out of every N clock cycles of a processor clock.

11. The method of claim 8, further comprising returning to the normal mode of operation after a predetermined time period has elapsed.

12. The method of claim 8, further comprising returning to the normal mode of operation when an event occurs.

13. The method of claim 8, further comprising running only one thread on the processor.

14. The method of claim 8, further comprising lowering processor voltage.

15. The method of claim 8, further comprising loading counters associated with the threads with a value to indicate how long the associated thread is to remain paused.

16. The method of claim 8, further comprising leaving the slow mode of operation and entering a slower mode of operation in response to a determination that the processor has been in the slow mode for a predetermined time period.

17. A method, comprising:

receiving a pause instruction from each thread running on a processor; and

hinting the processor to enter a low power mode in response to receiving the pause instruction from each thread running on the processor.

18. The method of claim 17, further comprising hinting the processor to remain in the low power mode for a predetermined time period.

19. The method of claim 17, further comprising hinting the processor to remain in the low power mode until an event occurs.

20. The method of claim 17, further comprising hinting the processor to enter a lower power mode after a predetermined time period elapses.

21. The method of claim 17, further comprising reducing a processor clock frequency.

22. The method of claim 17, further comprising lowering a processor voltage.

23. The method of claim 17, further comprising gating M clock cycles out of every N clock cycles of a processor clock.

24. An article of manufacture including a machine-accessible medium having data that, when accessed by a machine, cause the machine to perform the operations comprising:

receiving a pause instruction from each thread running on a processor; and

hinting the processor to enter a low power mode in response to receiving the pause instruction from each thread running on the processor.

25. The article of manufacture of claim 24, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising hinting the processor to remain in the low power mode for a predetermined time period.

26. The article of manufacture of claim 24, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising hinting the processor to remain in the low power mode until an event occurs.

27. The article of manufacture of claim 24, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising hinting the processor to enter a lower power mode after a predetermined time period elapses.

28. The article of manufacture of claim 24, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising reducing a processor clock frequency.

29. The article of manufacture of claim 24, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising lowering a processor voltage.

30. The article of manufacture of claim 24, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising gating M clock cycles out of every N clock cycles of a processor clock.